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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,894	08/28/2001	Christoph Dominique Loeffler-Lejeune	BAY-007	7829

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EXAMINER	
HAN, CLEMENCE S	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 11/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,894	LOEFFLER-LEJEUNE, CHRISTOPH DOMINIQUE	
	Examiner	Art Unit	
	Clemence Han	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,8,10,11,13-16,19,27 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15,16 and 28* is/are allowed.

6)☒ Claim(s) *1-5,7,8,10,11,13,14,19 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claim 1-5, 7, 8, 10, 11, 13, 14, 19 and 27 are rejected under 35 U.S.C. 102(a) as being anticipated by Sawey et al. (US Pub. 2002/0118668).

Regarding to claim 1, Sawey teaches an integrated circuit comprising: a first input port 850 a for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries; a second input port 860 for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries; a first frame position register (502 in 850) whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and a second frame position register (502 in 860) whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time; a controller configured to synchronize the first and second time-division multiplexed signals in response to the contents of the first and second frame position registers, wherein the controller is configured to generate first and second port-specific offset values 820 in

response to the contents of both the first and second frame position registers [0067]-[0070].

Regarding to claim 2, Sawey teaches a first memory (506 in 850) that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer (504 in 850) and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer (508 in 850); and a second memory (506 in 860) that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer (504 in 860) and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer (508 in 860).

Regarding to claim 3, Sawey teaches a first retimer (516, 522 in 850) for retiming said first time-division multiplexed signal; and a second retimer (516, 522 in 860) for retiming said second time-division multiplexed signal.

Regarding to claim 4, Sawey teaches an output port 300; and a cross-connect 14 for outputting at least a portion of said first time-division multiplexed signal via said output port.

Regarding to claim 5, Sawey teaches a method comprising: receiving a first time-division multiplexed signal that comprises a first series of frame boundaries 850; receiving a second time-division multiplexed signal that comprises a second

series of frame boundaries 860; indicating, at a point in time, how far said first time-division multiplexed signal is from a frame boundary (502 in 850); and indicating, at said point in time, how far said second time-division multiplexed signal is from a frame boundary (502 in 860); storing said first time-division multiplexed signal into a first memory (506 in 850) at a location that is indicated by a first write pointer (504 in 850); reading said first time-division multiplexed signal from a location in said first memory that is indicated by a first read pointer (508 in 850); storing said second time-division multiplexed signal into a second memory (506 in 860) at a location that is indicated by a second write pointer (504 in 860); and reading said second time-division multiplexed signal from a location in said second memory that is indicated by a second read pointer (508 in 860); and adjusting the first and second read pointers in response to first and second port-specific offset values 820 that are generated in response to the indication of how far both the first and second time-division multiplexed signals are from their respective frame boundaries at said point in time [0067]-[0070].

Regarding to claim 7, Sawey teaches retiming (516, 522 in 850) said first time-division multiplexed signal in accordance with a clock signal 510; and retiming (516, 522 in 860) said second time-division multiplexed signal in accordance with said clock signal.

Regarding to claim 8, Sawey teaches an apparatus comprising: a first integrated circuit comprising: (i) a first input port 850 for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries; (ii) a second input port 860 for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries; (iii) a first frame position register (502 in 850) whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and (iv) a second frame position register (502 in 860) whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time; and a second integrated circuit comprising a controller 516, 522 for reading the contents of said first frame position register and said second frame position register; wherein said first integrated circuit further comprises: (v) a first memory (506 in 850) that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer (504 in 850) and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer (508 in 850); and (vi) a second memory (506 in 860) that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer (504 in 860) and that reads said second time-division multiplexed signal at

a location that is indicated by a second read pointer (508 in 860); and wherein said controller 516, 522 is further configured to: store a value in said first read pointer (508 in 850) based on the contents of said first frame position register and said second frame position register [0058]; synchronize the first and second time-division multiplexed signals in response to the contents of the first and second frame position registers, generate first and second port-specific offset values 820 in response to the contents of both the first and second frame position registers; and adjust the first read pointer in response to the first port-specific offset value and the second read pointer in response to the second port-specific offset value [0067]-[0070].

Regarding to claim 10, Sawey teaches an output port 300; and a cross-connect 14 for outputting at least a portion of said first time-division multiplexed signal via said output port.

Regarding to claim 11, Sawey teaches a composite switch comprising: a first integrated circuit comprising: a first input port 850 for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries; a first frame position register (502 in 850) whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and a second integrated circuit

comprising: a second input port 860 for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries, and a second frame position register (502 in 860) whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time; and a controller 516, 522 configured to : read the contents of said first frame position register and said second frame position register; synchronize the first and second time-division multiplexed signals in response to the contents of the first and second frame position registers by; generating first and second port-specific offset values 820 in response to the contents of both the first and second frame position registers; and adjusting the first read pointer in response to the first port-specific offset value and the second read pointer in response to the second port-specific offset value [0067]-[0070].

Regarding to claim 13, Sawey teaches a first memory (506 in 850) that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer (504 in 850) and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer (508 in 850); and a second memory (506 in 860) that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer (504 in 860) and that

reads said second time-division multiplexed signal at a location that is indicated by a second read pointer (508 in 860).

Regarding to claim 14, Sawey teaches said controller 516, 522 is further for storing a value in said first read pointer (508 in 850) based on the contents of said first frame position register and said second frame position register [0058], [0067].

Regarding to claim 19, Sawey teaches the controller is further configured to adjust first and second read pointers in response to the first and second port-specific offset values 820, respectively [0058], [0067].

Regarding to claim 27, Sawey teaches a composite switch comprising: a first integrated circuit comprising: a first input port 850 for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries; a second input port 860 for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries, a first frame position register (502 in 850) whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time; and a second frame position register (502 in 860) whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time; a first memory (506 in 850) that stores said first time-division multiplexed signal at a

location that is indicated by a first write pointer (504 in 850) and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer (508 in 850); a second memory (506 in 860) that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer (504 in 860) and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer (508 in 860); a controller 516, 522 configured to adjust the first and second read pointer in response to the contents of the first and second frame position registers in order to synchronize the first and second time-division multiplexed signals [0067]-[0070]; and first and second frame position counters 502 configured to count the numbers of word of said respective first and second time-division multiplexed signals received since a frame boundary.

Allowable Subject Matter

3. Claim 15, 16 and 28 are allowed.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (571) 272-3158. The examiner can normally be reached on Monday-Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C. H.

Clemence Han
Examiner
Art Unit 2616

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